WHAT IS CLAIMED IS:

1. A flip chip packaging process comprising:

providing a wafer having a plurality of chips formed thereon, wherein each chip has an active surface provided with a plurality of bonding pads;

forming a bump on each bonding pad;

providing a plurality of substrates, wherein each substrate includes at least a package unit, each package unit having a plurality of contact pads thereon;

respectively mounting the substrates onto the wafer such that each package unit corresponds to each chip and the contact pads are respectively connected to the corresponding bumps, wherein two neighboring substrates are separated by a gap;

filling an underfill material between the substrates and the wafer, the underfill material being introduced through the gaps between the substrates and from the boundary of the wafer;

solidifying the underfill material; and

dicing the wafer and the substrates to form a plurality of individualized packages, each individualized package including one chip and one package unit.

2. The flip chip packaging process of claim 1, wherein each substrate includes at least a patterned conductive layer alternately laminated with at least an insulating layer.

3. The flip chip packaging process of claim 1, wherein each substrate includes a plurality of patterned conductive layers alternately laminated with a plurality of insulating layers.

4. The flip chip packaging process of claim 2, wherein the material of the insulating layer is FR-4, FR-5, bismaleimide triazine (BT), polyimide, or materials composite of epoxy and ceramic.

5. The flip chip packaging process of claim 1, wherein the material of the bumps is tin-lead alloy, gold or conductive polymer.

6. The flip chip packaging process of claim 1, wherein the surface of each of package unit is smaller or equal to the active surface of the corresponding chip.

7. A flip chip packaging process comprising:

providing a wafer having a plurality of chips formed thereon, wherein each chip has an active surface provided with a plurality of bonding pads;

providing a plurality of substrates, wherein each substrate includes at least a package unit, the package unit having a plurality of contact pads;

forming a bump on each contact pad;

respectively mounting the substrates onto the wafer such that each package unit corresponds to one chip and the bonding pads are respectively connected to the corresponding bumps, wherein two neighboring substrates are separated by a gap;

filling an underfill material between the substrates and the wafer, wherein the underfill material is introduced through the gaps between the substrates and from the boundary of the wafer;

solidifying the underfill material; and

dicing the wafer and the substrates to form a plurality of individualized packages, each individualized package including one package unit and one chip.

8. The flip chip packaging process of claim 7, wherein each substrate includes by at least a patterned conductive layer alternately laminated with at least an insulating layer.

9. The flip chip packaging process of claim 7, wherein each substrate includes a plurality of patterned conductive layers alternately laminated with a plurality of insulating layers.

10. The flip chip packaging process of claim 8, wherein the material of the insulating layer is FR-4, FR-5, bismaleimide triazine (BT), polyimide, or materials composite of epoxy and ceramic.

11. The flip chip packaging process of claim 7, wherein the material of the bumps is tin-lead alloy, gold or conductive polymer.

12. The flip chip packaging process of claim 7, wherein the surface of each package unit is smaller or equal to the active surface of the corresponding chip.